AMENDMENTS TO THE SPECIFICATION

1. Please amend paragraph [0035] as follows:

[0035] At the same time, the phase signal PM2 is also applied to the phase offset **523** for the fractional-N PLL modulation **500** that is used to track the carrier frequency of VCO **521**. In operation, a modulated signal from the loop filter **517** is coupled to the adder **519** such that the VCO **521** operates with two signals. By using the feed-forward phase modulation through the D/A converter **513**, a change in the phase gain value will result in an equivalent change in the modulation gain of VCO **521**. Thus, the nonlinear effect of VCO gain drift can be adaptively compensated by predistorting the scaling value of the phase gain **511**. Also, a controller **524** receives the phase-modulated baseband signal and the carrier frequency signal to produce a ~~digital bit stream used~~ signal to control a reference frequency coupled to an input of the phase detector **515**.

2. Please amend paragraph [0037] as follows:

[0037] According to one embodiment, the fractional-N phase-locked loop (PLL) frequency synthesizer **500** is used as a functional building block in the transmitter **580**. The phase-locked loop **500** includes a phase detector **515**, a loop filter **517**, a voltage controlled oscillator (VCO) **521** and a loop divider **525**. The phase detector **515** serves as a comparator ~~means~~ for comparing the signal from the controller **524** ~~reference signal f_{ref}~~ to the divided loop output signal ~~which is coupled to the output of~~ from the divider **525**. The phase detector **515** generates a frequency tuning control signal that is coupled to the loop filter **517**. The voltage level of this frequency tuning control signal is proportional to the difference in frequencies of the compared signals. The loop filter **517** receives and filters the frequency tuning control signal and provides a control signal to the input node **519** to the VCO **521**. The VCO **521** serves as a frequency generation means for generating the loop output signal f_{out} in response to the VCO input control signal. The loop divider **525** is coupled to the output of the VCO **521** and generates a divided loop signal which corresponds to the frequency to the loop output signal divided by integer N or N+1. The output of the

loop divider **525** is provided as the loop feedback signal to the other input of phase detector **515**.